REMARKS

Reconsideration and further examination of the application, as amended, are respectfully requested.

In the Office Action, claims 1, 4-6, 9 and 10 were rejected under 35 U.S.C. §103 based on U.S. Patent No. 5,963,745 to Collins et al. ("Collins") in view of U.S. Patent No. 5,815,723 to Wilkinson et al. ("Wilkinson I"). Claims 2, 3, 7 and 8 were rejected under §103 based on Wilkinson I in view of U.S. Patent No. 5,878,241 to Wilkinson et al. ("Wilkinson II"). Applicants respectfully traverse the rejection.

System Claim 1, in relevant part, recites:

> "A multiprocessor computer system having a plurality of processors interconnected so that they can share memory, comprising"
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> "a plurality of links, each link of said plurality of links connecting a processor to another processor",
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> "a plurality of microprocessors, each of said microprocessors having a microprocessor memory associated therewith, **a selected microprocessor** of said plurality of microprocessors **associated with at least one processor** of said plurality of processors, **said plurality of microprocessors arranged to control said plurality of processors**, said control including applying electric power to a selected processor and removing electric power from said selected processor", and
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> "a data structure stored in microprocessor memory, said data structure storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links, a copy of said data structure stored in microprocessor memory of each of said microprocessors".

Applicants direct the Examiner's attention to Figs. 8-10, which illustrate a preferred embodiment of the present invention. As shown, each EV7 processor 860 is pref-

erably coupled, e.g., via serial links 820, to a microprocessor-based CPU Management Module (CMM) 810. The CMM 810, moreover, provides power and initialization control to its respective EV7 processor 860. See Specification at pp. 14 and 22. Based upon Applicants' review of Collins, that reference fails to teach or suggest such a plurality of microprocessors arranged to control the processors of a multiprocessor computer system.

Collins discloses a memory chip array processor, which Collins calls its Advanced Parallel Array Processor (APAP). See Col. 11, lines 65-66. Each ADAP chip has 8 identical processor memory elements (PMEs) and one broadcast and control interface (BCI). Col. 26, lines 27-30. Each PME, moreover, "is a powerful microcomputer having significant memory and I/O functions". Col. 15, lines 41-42. By combining together a plurality of these APAP chips, Collins can create a massively parallel computer system. Col. 11 lines 38-42.

The Office Action states that Collins at Col. 7, lines 8-37 discloses the claimed "plurality of microprocessors", that Col. 15, lines 60-62 discloses the claimed "a selected microprocessor . . . associated with at least one processor", and that Fig. 18 and Col. 3, line 64 to Col. 4, line 24 disclose the claimed "said plurality of microprocessors arranged to control the plurality of processors". Applicants respectfully disagree that the cited portions of Collins support such a reading.

First, Col. 7, lines 8-37 is an excerpt from Collins' Glossary of Terms that provides an explanation of the following terms: "Picket Chip", "Picket Processor system", "Picket Architecture", "Picket Array", and "PME". According to Collins, moreover, the term PME means "a single processor, memory and I/O capable system element or unit

that **forms one of our parallel array processors**". In other words, with Collins, the term "PME" refers to a primary or main processor of a massively parallel computer. It does not refer to a microprocessor that is both associated with a main processor, and is arranged to control that processor, as recited in claim 1. Because Collins' PME is directed to its main processor element, it is improper for the Office Action to contend that the PME is a separate microprocessor used for controlling the plurality of processors of a multiprocessor computer system.

Second, Col. 15, lines 60-62 provides no teaching or suggestion for associating a selected microprocessor with at least one of the main processors of the multiprocessor system. Instead, this excerpt describes how different "select groups" of Collins' PMEs can be established to solve difficult processing tasks, such as executing complex math functions or generating 3-D image displays.

Third, Col. 3, line 65 to Col. 4 line 24 provides no teaching or suggestion for a plurality of microprocessors arranged to control a plurality of processors of a multiprocessor computer system. Like the excerpt mentioned above, this excerpt is from Collins' Glossary of Terms. The terms being defined in this excerpt are: "Cluster", "Cluster controller", "Cluster synchronizer" and "Controller". Collins' definition of "Controller" is as follows:

> A controller is a device that directs the transmission of data and instructions over the links of an interconnection network: its operation is controlled by a program executed by a processor to which the controller is connected or by a program executed within the device.

There is no teaching or suggestion for a microprocessor that is associated with a processor of a multiprocessor computer, and is also arranged to control that processor. Instead, by "controller", Collins is referring to a device that deals with the transmission of data and instructions over inter-communication links.

Finally, it is improper for the Office Action to say, in the first instance, that Collins' PMEs correspond to the claimed "plurality of microprocessors", but then to later contend that it is not the PMEs at all, but rather Collins' definition of the term "controller" that corresponds to the claimed plurality of microprocessors. Collins itself provides no justification for doing so, and no justification is provided in the Office Action. Because Collins fails to teach or suggest Applicants' "plurality of microprocessors that are associated with the processors of the multiprocessor system and arranged to control those processors," the rejection of claim 1 should be withdrawn.

The Office Action further states that Wilkinson, in the Abstract and at Cols. 4 and 19, teaches or suggests Applicants' claimed "data structure . . . storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links". Applicants respectfully disagree.

In the Abstract, Wilkinson simply states that each processing element of its parallel array computer has "a processor coupled with a local memory". There is no mention by Wilkinson of some data structure storing a representation of the links connecting the processors of a multiprocessor computer system.

Col. 4, lines 19-24, of Wilkinson correspond to an excerpt of a Glossary of Terms. The word being defined in this excerpt is CMOS. Specifically, Wilkinson notes that

CMOS is a common fabrication technique for Dynamic Random Access Memories (DRAMs). There is no mention by Wilkinson in this excerpt of some data structure storing a representation of the links connecting the processors of a multiprocessor computer system.

At Col. 19, lines 3-8, Wilkinson states that a host processor can load microcode programs into an array controller, exchange data with the array controller and monitor the array controller's status. Again, there is no mention by Wilkinson of some data structure storing a representation of the links connecting the processors of a multiprocessor computer system.

Thus, Wilkinson fails to teach or suggest Applicants' claimed "data structure for storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links".

As claims 2-5 depend from claim 1, the rejections of these claims should also be withdrawn.

Method claim 6, in relevant part, recites:

> "interconnecting a plurality of microprocessors, each of said microprocessors having a microprocessor memory associated therewith, **a selected microprocessor** of said plurality of microprocessors **associated with at least one processor** of said plurality of processors, **said plurality of microprocessors arranged to control said plurality of processors**, said control including applying electric power to a selected processor and removing electric power from said selected processor" and
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> "storing a data structure in microprocessor memory, said data structure storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links, a copy of said data structure stored in microprocessor memory of each of said microprocessors".

As shown, claim 6, like claim 1, recites a selected microprocessor being associated with one of the processors of the multiprocessor system, and the microprocessors being arranged to control the processors of the multiprocessor system. Thus, claim 6 is distinguishable over Collins for the reasons set forth above.

Claim 6 also recites "storing a data structure representing the links connecting the processors". As described above, Wilkinson fails to teach or suggest such a feature. Claim 6 is thus distinguishable over the art of record for this reason as well.

Claims 7-10 depend from claim 6 and thus the rejection of these claims should also be withdrawn.

Applicants have amended the Specification to add the Serial Numbers of the cross-related applications, which were not available at the time the present application was filed. Applicants have also amended the claims to correct several minor terminology errors, and to provide a proper antecedent basis for the claimed elements. No new matter is being introduced.

Applicants submit that the application as amended is in condition for allowance and early favorable action is requested.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

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